

FIGURE 1.

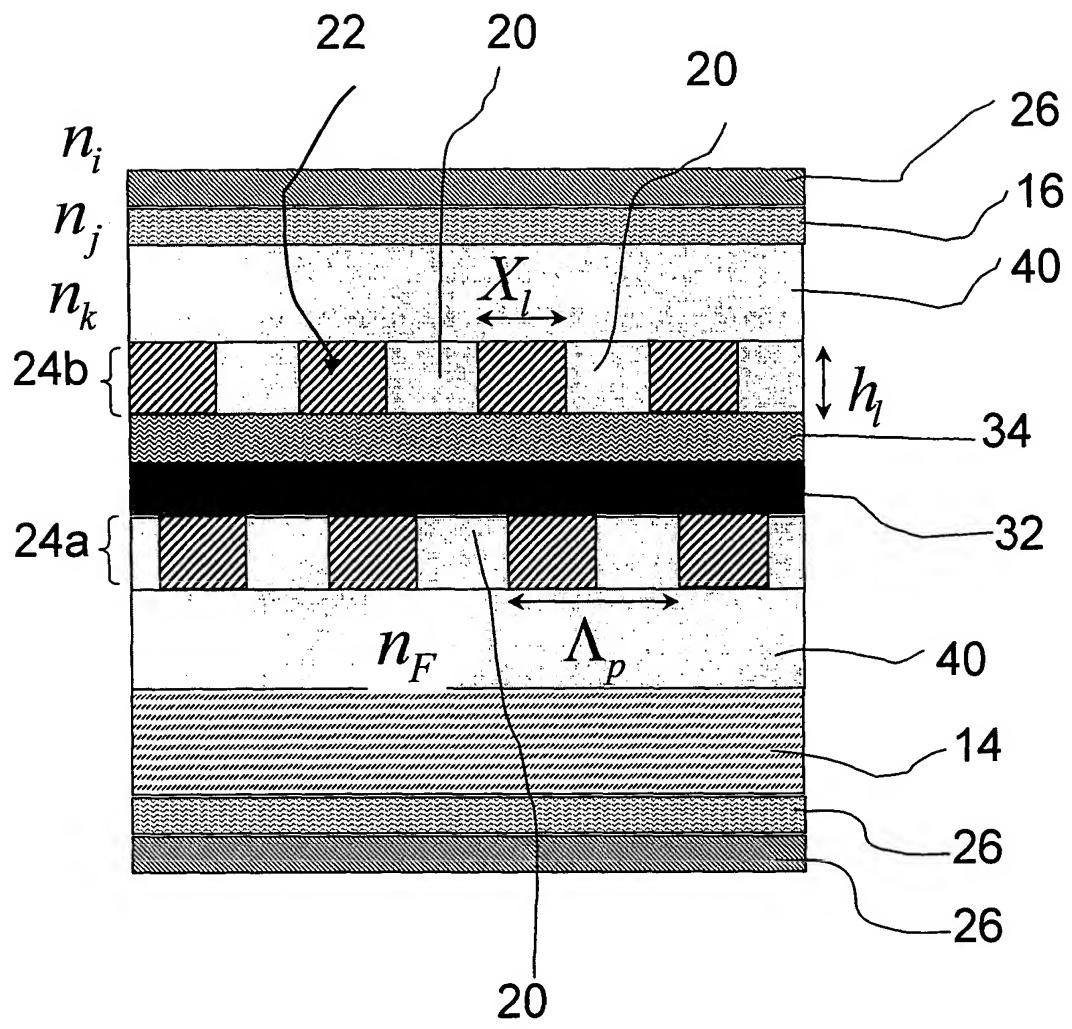


FIGURE 2.

Design, simulation of structures



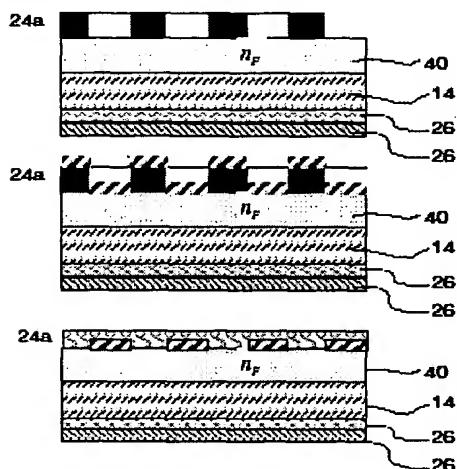
Substrate preparation with appropriate layers



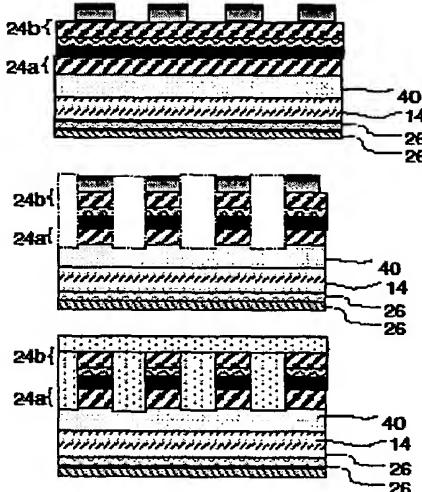
Patterning of first functional layer(s)

Nanoimprint, photolithography, e-beam lithography, holography

Addition methods



Subtraction methods

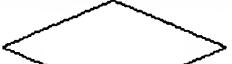


In-process monitor, characterization, metrology, etc



Performance assessments

Negative, ABORT ?



Positive

Add additional buffer layer(s), etching stop layer(s), and/or coupling layer(s)



Additional patterning of the layer(s)



FIGURE 3.

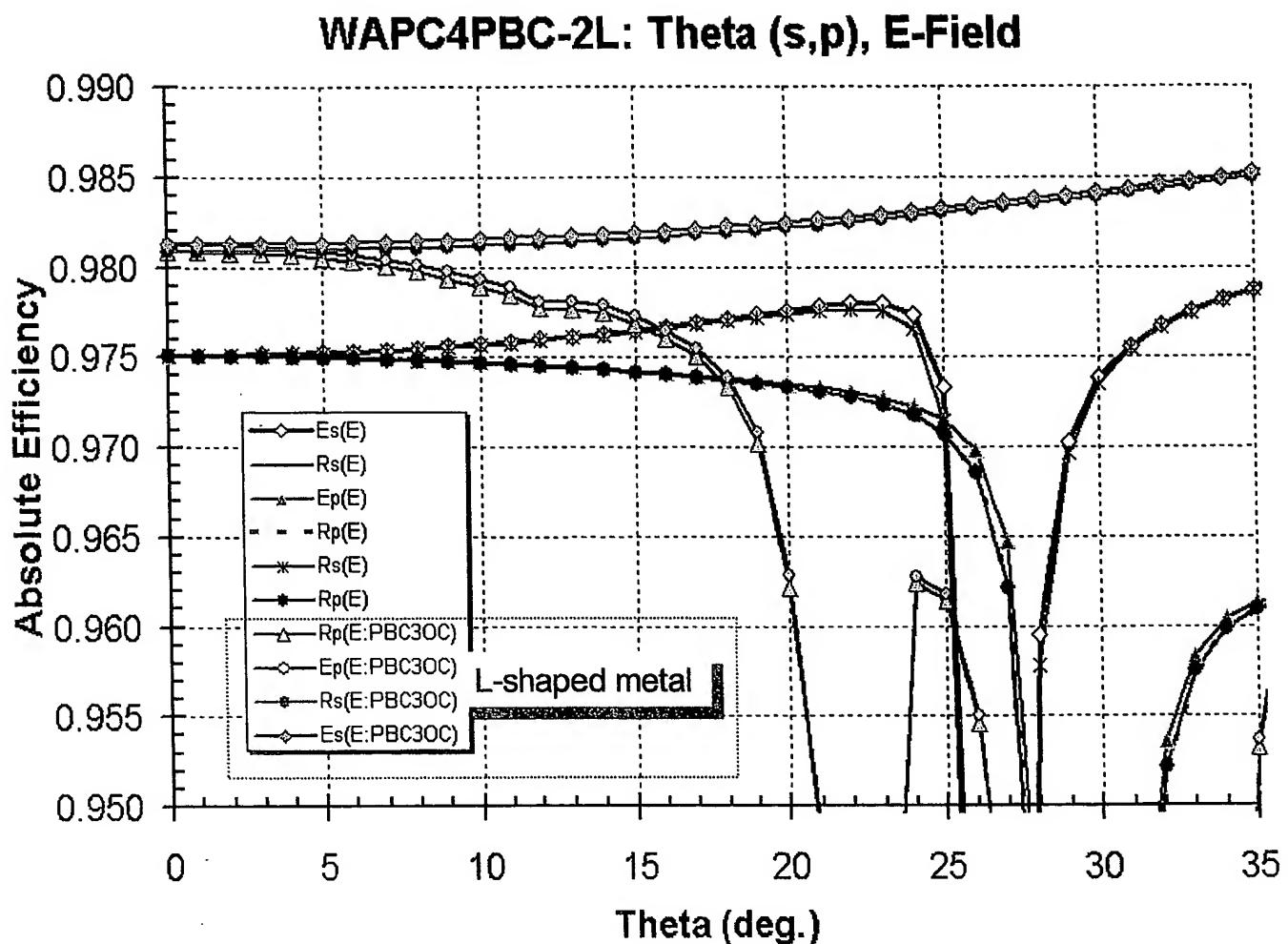


Figure 4

WAPC4PBC-2L: Theta (s,p), M-Field

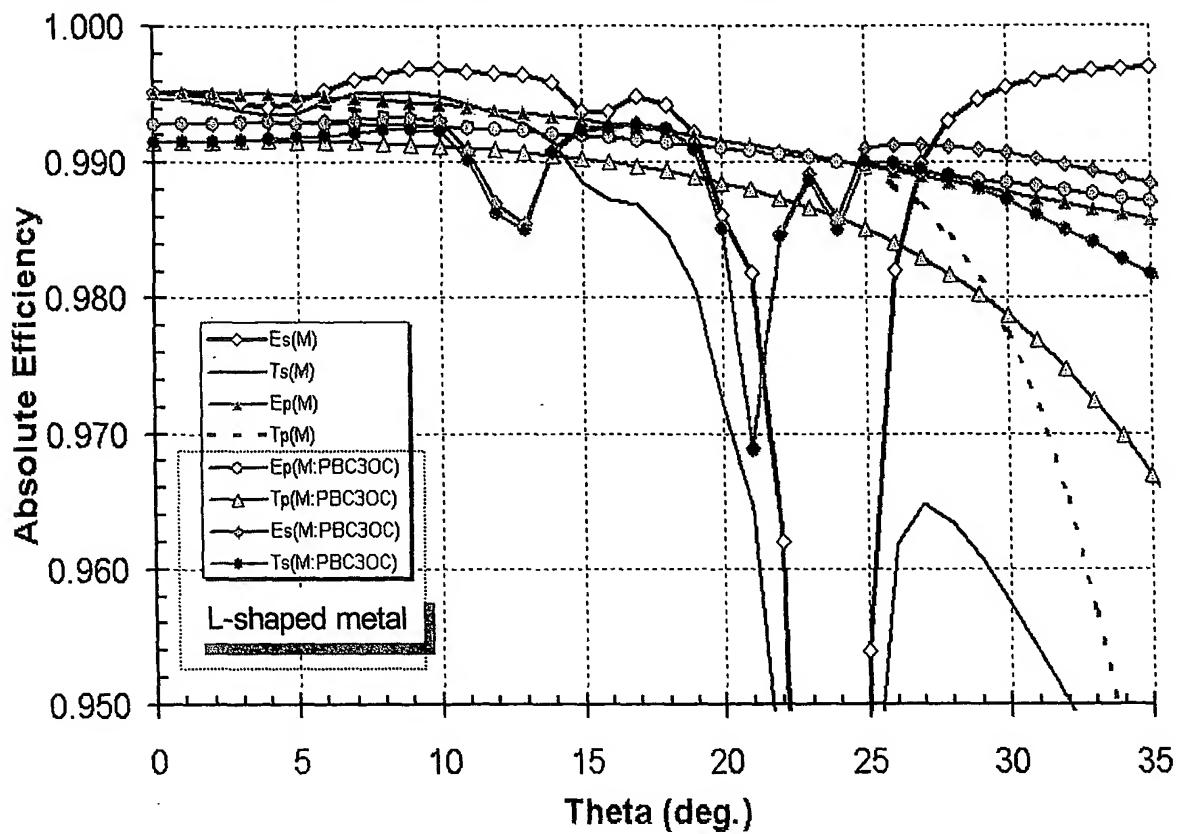


Figure 5

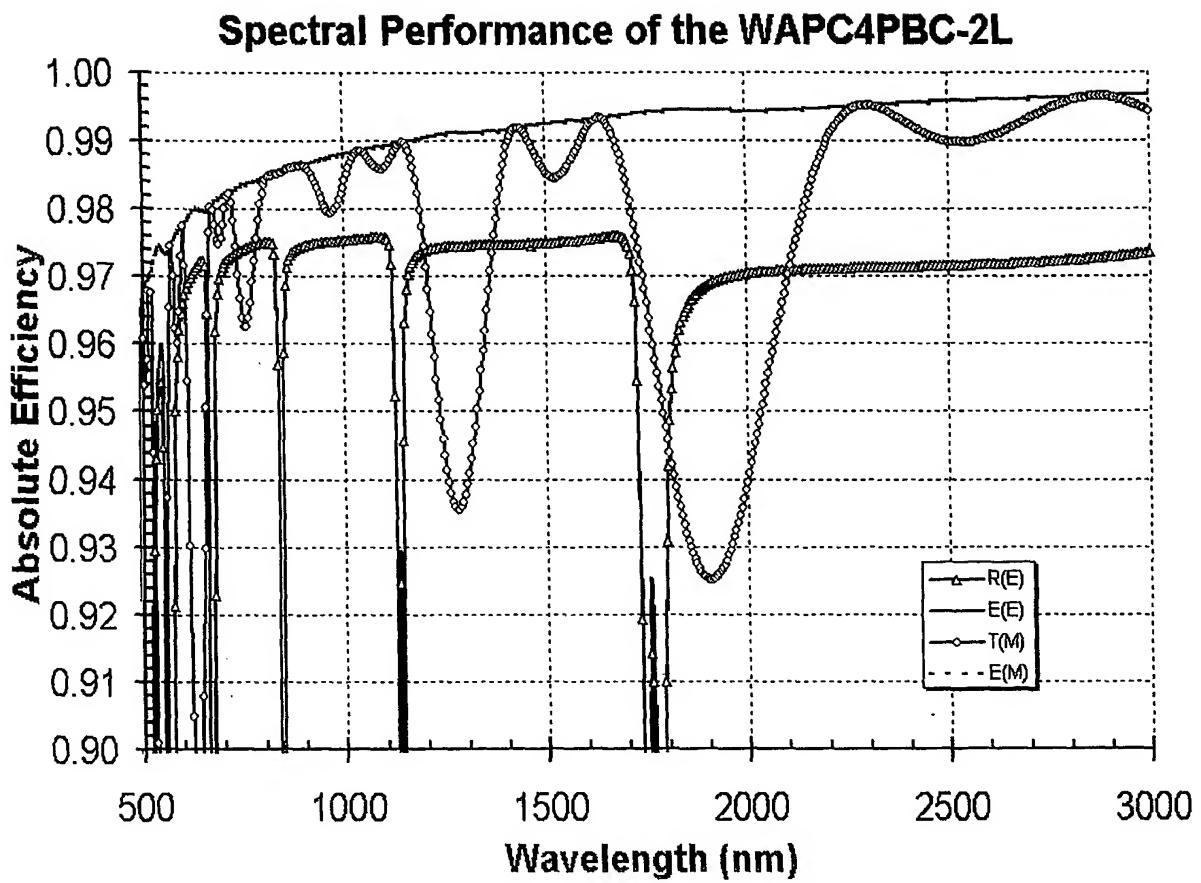


Figure 6

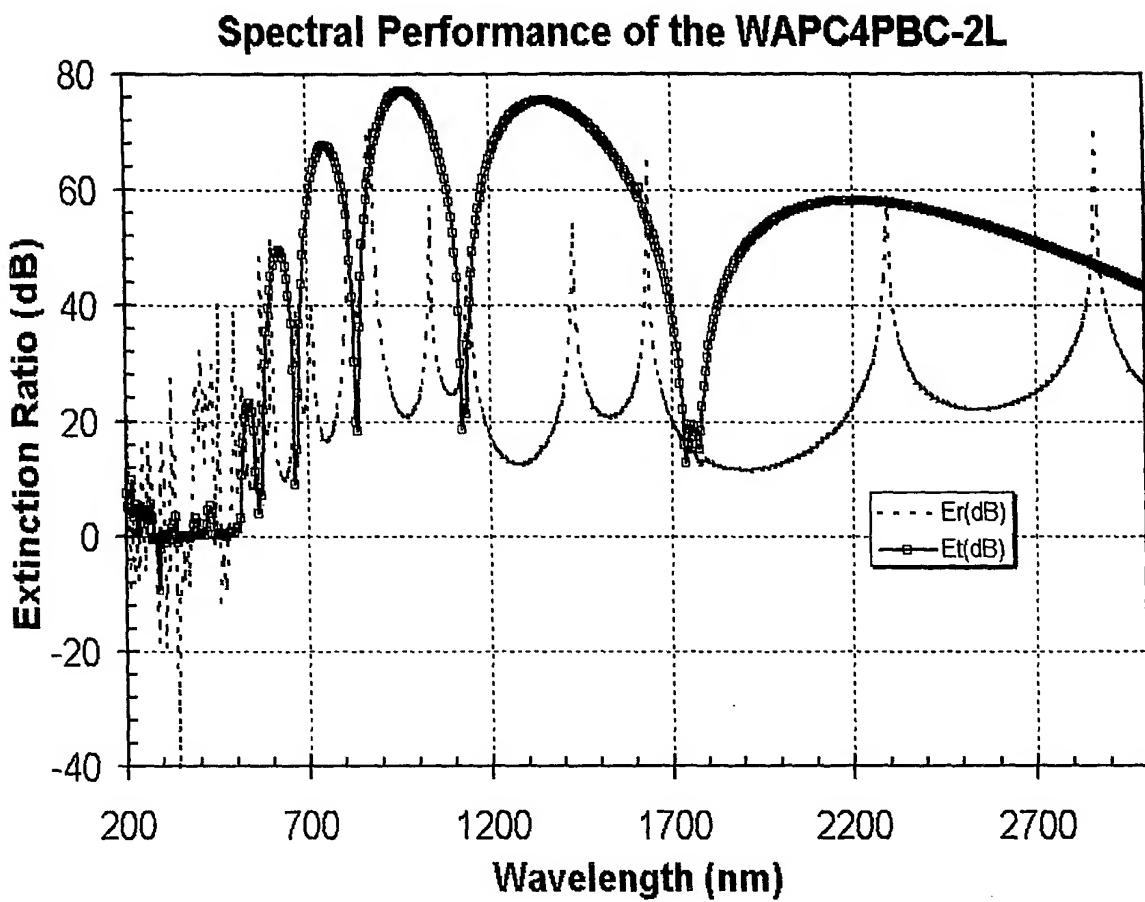


Figure 7

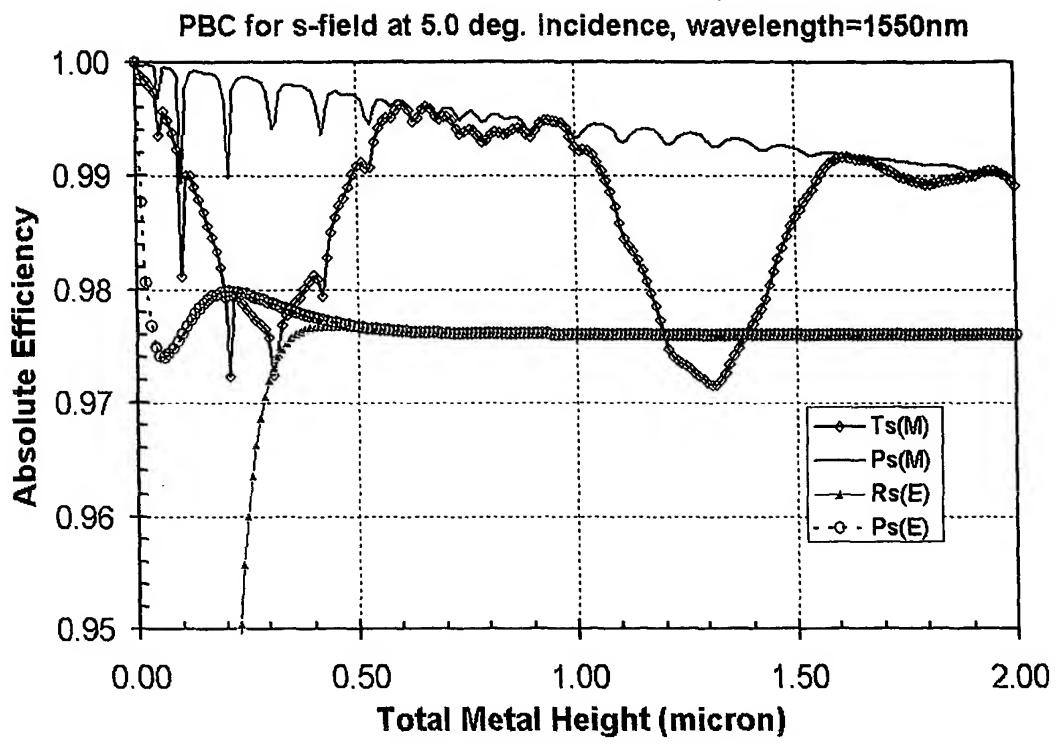


Figure 8A

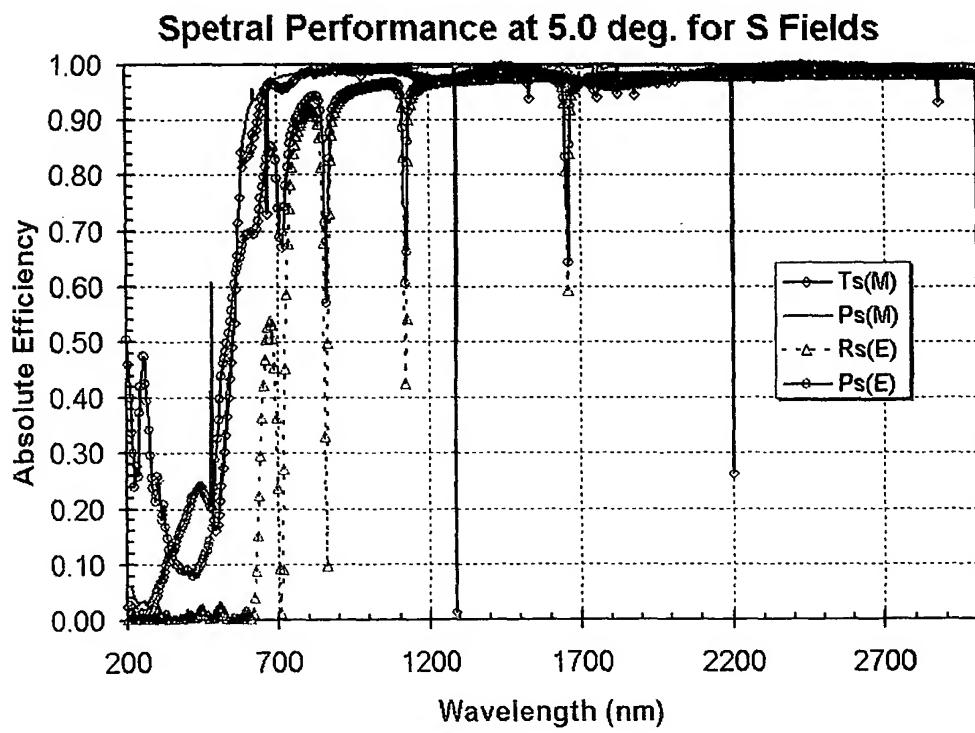


Figure 8B

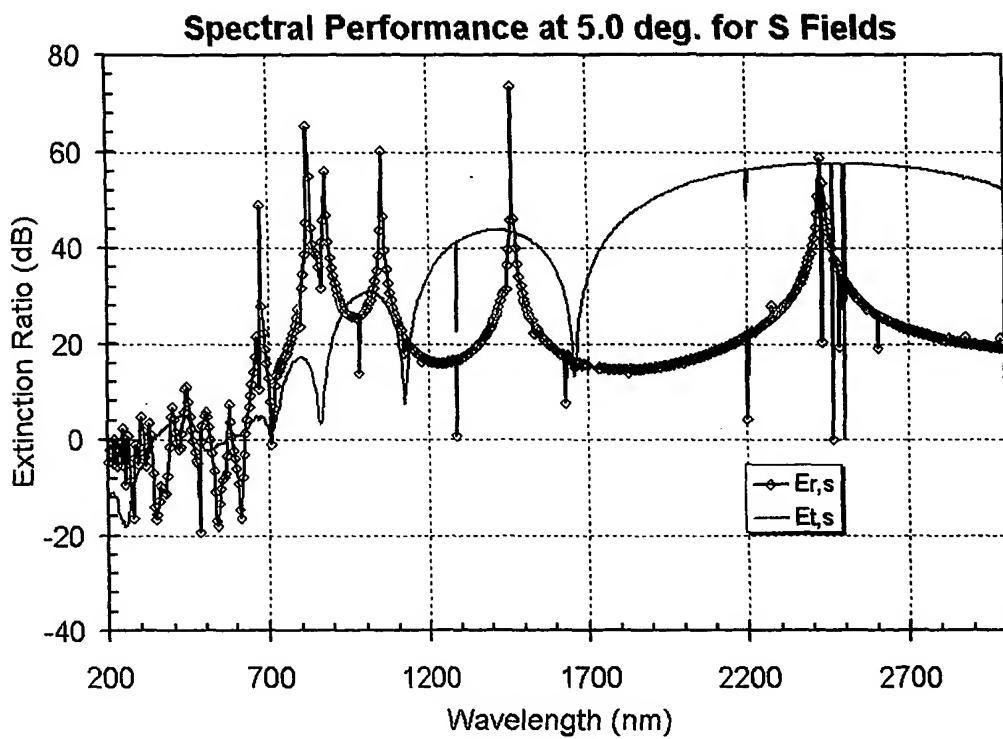


Figure 8C

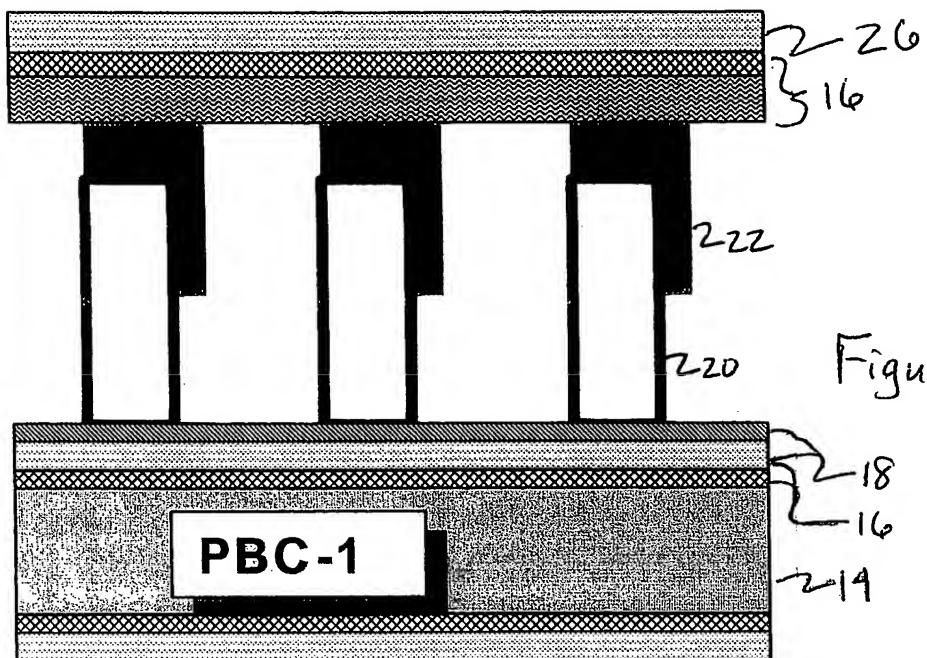


Figure 9A

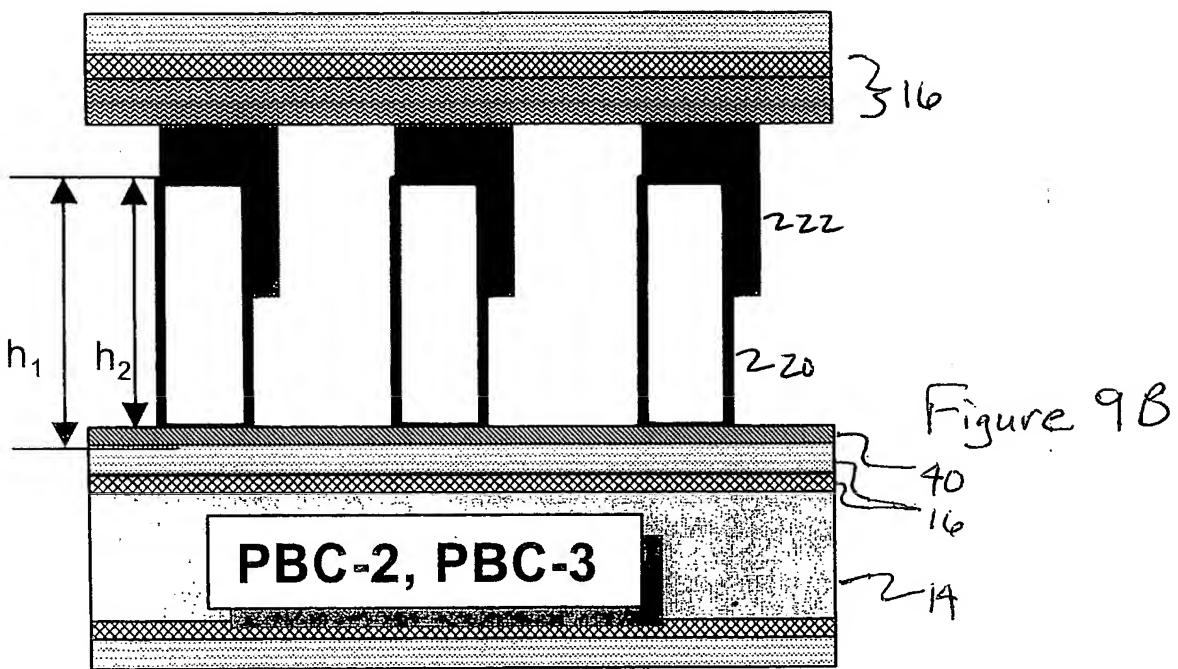


Figure 9B

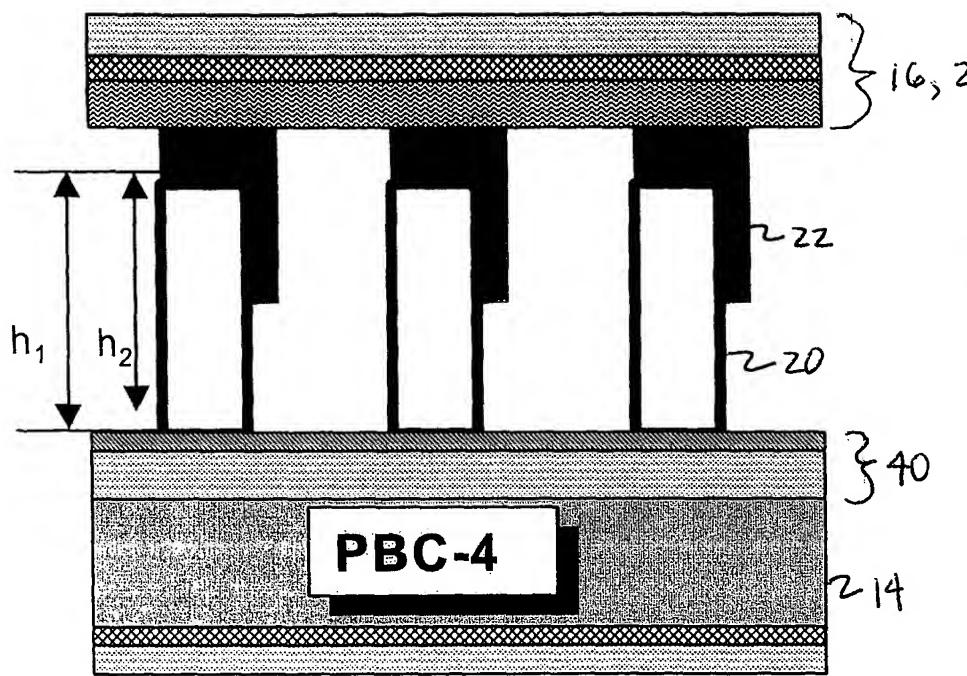


Figure 9C

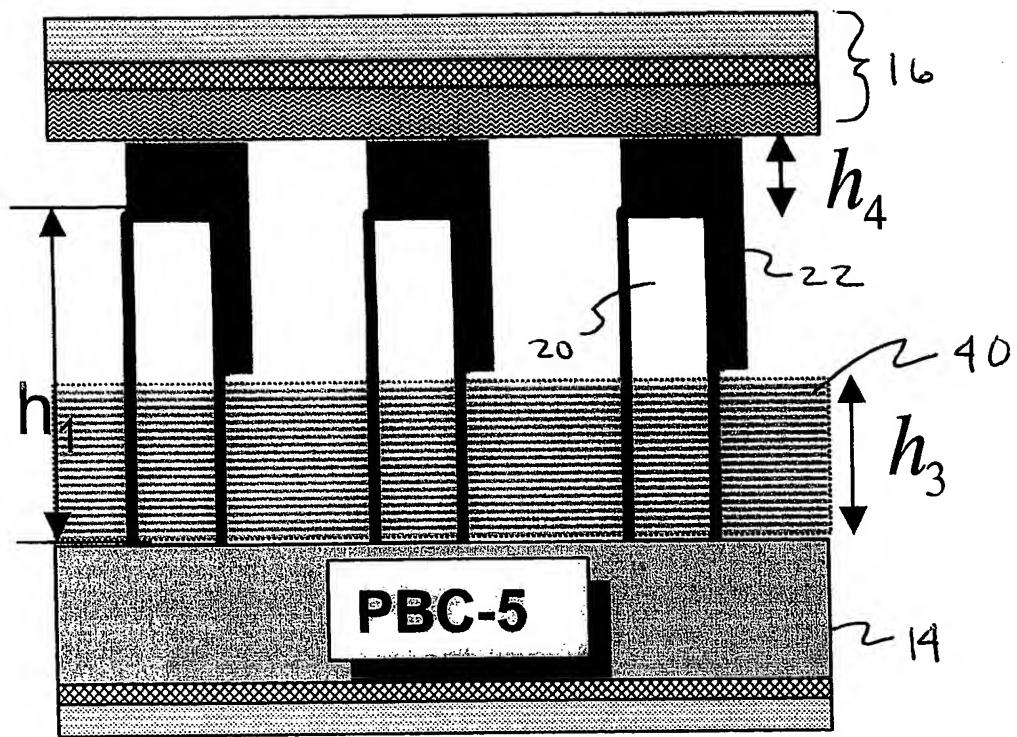


Figure 9 D

Performance of SOE's

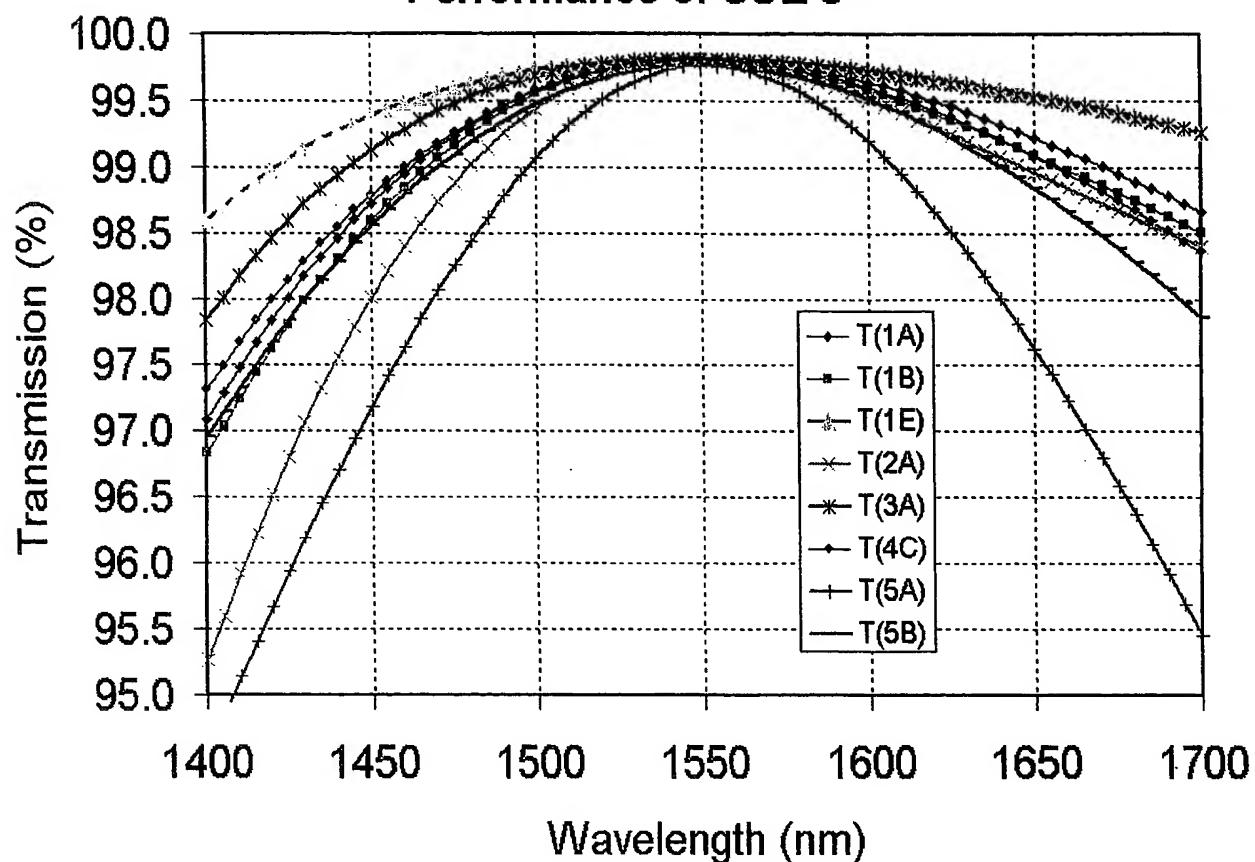


Figure 10